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10/734,117	12/15/2003	Daniel Yellin	MP1493 151668	4852

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EXAMINER	
AGHDAM, FRESHTEH N	
ART UNIT	**PAPER NUMBER**
2611	
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06/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/734,117	YELLIN ET AL.	
	Examiner	Art Unit	
	Freshteh N. Aghdam	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14,15,18,19,22 and 26-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12, 14-15, 18-19, 22 and 26-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 5/8/2007 have been fully considered but they are not persuasive.

Applicant's Argument(s): Regarding claims 1-32, the applicant argues that the claimed invention is not taught or suggested by Vilcocq "wherein digital values of said pre-emphasis filter are to be adjusted so that said transfer function is optimized according to predefined optimization criteria; and wherein said optimization criteria includes a mean squared error of an input to said pre-emphasis filter and an input to a voltage controlled oscillator of said fractional-N phase locked loop unit."

Examiner's Response: Regarding the argument set forth above, examiner respectfully disagrees with the applicant because the pre-emphasis filter of Vilcocq's is an adaptive filter (an adaptive filter by definition is a filter whose transfer function is adjusted according to an optimization criteria until the optimization criteria is satisfied) that is based on **two inputs** (Fig. 2, means 26, Pmod (inputted to the pre-emphasis filter through phase/frequency conversion); Smodn (comes from the output of the PLL); Par. 12-13 and 54), wherein the optimization criteria includes a mean squared error of an input to the pre-emphasis filter through the phase/frequency converter and an output to the PLL in which the output to the PLL includes **the output to the VCO in addition to the input to the VCO**. Therefore, the optimization criteria includes a mean squared

error of an input to the pre-emphasis filter and an input to a voltage controlled oscillator of the PLL.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 10-13; and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vilcocq et al (US 2004/0041638).

As to claim 1, Vilcocq discloses a method comprising building a linear model of an analog fractional-N phase locked loop unit including a bilinear model of loop filter of the phase locked loop, wherein the analog fractional-N phase locked loop includes a voltage controlled oscillator (Fig. 2, means 11-14; Par. 33-37 and 40-45); and determining a transfer function of a filter that is optimized according to predefined optimization criteria (Par. 12-13 and 54-55) to determine the pre-emphasis filter, wherein the optimization criteria is related to an input to said pre-emphasis filter and an output to the voltage controlled oscillator (Fig. 2; Par. 12-13 and 40-45). Vilcocq is not explicit about the optimization criteria relate to an input to said filter and an input to the voltage-controlled oscillator. One of ordinary skill in the art would recognize that optimization criteria of Vilcocq not only relate to the input of the voltage-controlled oscillator (i.e. output of the loop filter) but also relate to the input to the voltage-

controlled oscillator. Therefore, it would have been obvious to one of ordinary skill in the art to improve the system performance of the digital synthesizer by adapting the transfer function of the filter to the linearized response of the phase locked loop variations.

As to claim 2, Vilcocq discloses that said model includes impairments of one or more components of the phase locked loop (Par. 38-39).

As to claim 3, Vilcocq discloses that the model includes phase noise (Par. 12-13).

As to claim 4, Vilcocq discloses that the model includes variations of parameters of phase locked loop unit from nominal values (Par. 38-39).

As to claim 5, Vilcocq discloses that determining the transfer function includes determining the transfer function to be optimized according to the predefined optimization criteria that includes a mean squared error of an input to the filter and an output to the voltage controlled oscillator (Par. 12-13).

As to claim 6, Vilcocq discloses determining the transfer function of the filter that is optimized based on performance characteristics (i.e. quality parameter(s)) estimation of the output of the voltage-controlled oscillator (Par. 12-13). Vilcocq is not explicit about determining the transfer function includes determining the transfer function to be optimized according to the predefined optimization criteria that includes spectral cleanliness of an output of the voltage controlled oscillator. However, one of ordinary skill in the art would recognize that spectral cleanliness of the voltage-controlled oscillator is a quality parameter. Therefore, it would have been obvious to one of ordinary skill in the art to optimize the transfer function of the filter based on spectral

cleanliness of the voltage-controlled oscillator in order to enhance performance of the digital modulation of a PLL synthesizer.

As to claim 7, Vilcocq inherently discloses selecting topology for the transfer function (Fig. 2, means 18, A(z)).

As to claim 10, Vilcocq discloses a method comprising adjusting digital values of a filter to compensate for variations in an analog fractional-N phase locked loop (Par. 7-13; Fig. 2, means 18); and determining adjusted digital values so that a transfer function of said pre-emphasis filter is optimized according to predefined optimization criteria, wherein the optimization criteria is related to an input to said pre-emphasis filter and an output to the voltage controlled oscillator (Fig. 2; Par. 12-13 and 54-55). Vilcocq is not explicit about the optimization criteria relate to an input to said filter and an input to the voltage-controlled oscillator. One of ordinary skill in the art would recognize that optimization criteria of Vilcocq not only relate to the input of the voltage-controlled oscillator (i.e. output of the loop filter) but also relate to the input to the voltage-controlled oscillator. Therefore, it would have been obvious to one of ordinary skill in the art to improve the system performance of the digital synthesizer by adapting the transfer function of the filter to the linearized response of the phase locked loop variations.

As to claim 11, Vilcocq discloses adjusting the digital values includes adjusting the digital values to compensate at least for variations in voltage, temperature, aging, or any combination thereof (Par. 38-39).

As to claim-12, Vilcocq discloses adjusting the digital values includes adjusting the digital values to compensate at least for variations of parameters of the phase locked loop unit from nominal values (Par. 38-39).

As to claim 13, Vilcocq discloses determining adjusted digital values so that a transfer function of the filter is optimized according to predefined optimization criteria (Par. 12-13).

As to claim 29, Vilcocq discloses a communication system comprising a receiver and a transmitter (Par. 1), wherein the transmitter including at least a fractional-N sigma-delta modulator (Fig. 2, means 15); an adaptive pre-emphasis filter coupled to an input of a sigma-delta modulator (means 18); and a fractional-N phase locked loop unit coupled to an output of the sigma-delta converter (means 11-14), wherein a transfer function of the adaptive pre-emphasis filter is to be optimized according to predefined optimization criteria, (Par. 8-13 and 54-55), wherein the optimization criteria is related to an input to said pre-emphasis filter and an output to the voltage controlled oscillator (Fig. 2; Par. 12-13 and 54-55). Vilcocq is not explicit about the optimization criteria relate to an input to said filter and an input to the voltage-controlled oscillator. One of ordinary skill in the art would recognize that optimization criteria of Vilcocq not only relate to the input of the voltage-controlled oscillator (i.e. output of the loop filter) but also relate to the input to the voltage-controlled oscillator. Therefore, it would have been obvious to one of ordinary skill in the art to improve the system performance of the digital synthesizer by adapting the transfer function of the filter by taking into the consideration the phase locked loop variations.

Claims 8-9, 14-15, 18-19, 22, and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vilcocq et al, and further in view of Perrott et al (US 6,008,703).

As to claims 8-9, Vilcocq discloses all the subject matter claimed in claim 1, except for the digital filter is a finite impulse response (FIR) or an infinite impulse response (IIR) filter. Perrott discloses digital modulation of a PLL synthesizer, wherein the filter can be an FIR or IIR filter (Col. 11, Lines 1-14) and the FIR transfer function is more preferred comparing to an IIR transfer function filter since the filter utilizing the FIR transfer function is implemented in a Read Only Memory; and also, it is well known in the art that FIR filter is more stable and have linear phase response. On the other hand, IIR filters utilize less number of taps than FIR filters. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Perrott with Vilcocq for the reasons stated above.

As to claim 14, Vilcocq discloses a fractional-N sigma-delta modulator comprising: a digital filter with a transfer function, the filter is coupled to an input of a sigma-delta converter (Fig. 2, means 15 and 18); and a fractional-N phase locked loop unit coupled to an output of the sigma-delta converter (means 11-14), wherein the optimization criteria is includes a mean squared error of an input to the pre-emphasis filter and output to the voltage controlled oscillator of the PLL (Fig. 2, Par. 12-13 and 54-55. Vilcocq is not explicit about the optimization criteria relate to an input to said filter and an input to the voltage-controlled oscillator. One of ordinary skill in the art would

recognize that optimization criteria of Vilcocq not only relate to the input of the voltage-controlled oscillator (i.e. output of the loop filter) but also relate to the input to the voltage-controlled oscillator. Therefore, it would have been obvious to one of ordinary skill in the art to improve the system performance of the digital synthesizer by adapting the transfer function of the filter to the linearized response of the phase locked loop variations. Also, Vilcocq is not explicit about the transfer function of the digital filter is a finite impulse response transfer function. Perrott discloses digital modulation of a PLL synthesizer, wherein the filter can be an FIR or IIR filter (Col. 11, Lines 1-14) and the FIR transfer function is more preferred comparing to an IIR transfer function filter since the filter utilizing the FIR transfer function is implemented in a Read Only Memory; and also, it is well known in the art that FIR filter is more stable and have linear phase response. On the other hand, IIR filters utilize less number of taps than FIR filters. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Perrott with Vilcocq for the reasons stated above.

As to claim 15, Vilcocq discloses that the transfer function is substantially equivalent to a transfer function of a minimum mean squared error equalizer (Par. 12-13).

As to claim 18, Vilcocq discloses determining the transfer function of the filter that is optimized based on performance characteristics (i.e. quality parameter(s)) estimation of the output of the voltage-controlled oscillator (Par. 12-13). Vilcocq is not explicit about determining the transfer function includes determining the transfer function to be optimized according to the predefined optimization criteria that includes spectral

cleanliness of an output of the voltage controlled oscillator. However, one of ordinary skill in the art would recognize that spectral cleanliness of the voltage-controlled oscillator is a quality parameter. Therefore, it would have been obvious to one of ordinary skill in the art to optimize the transfer function of the filter based on spectral cleanliness of the voltage-controlled oscillator in order to enhance performance of the digital modulation of a PLL synthesizer.

As to claim 19, Vilcocq discloses a fractional-N sigma-delta modulator comprising: a sigma-delta modulator (Fig. 2, means 15); a fractional-N phase locked loop unit coupled to an output of said sigma-delta modulator and including a voltage controlled oscillator (means 11-14); and a digital filter with a transfer function, the filter coupled to an input of the sigma-delta modulator, wherein the transfer function is not an inverse of a transfer from an output of the filter to an output of the voltage-controlled oscillator (Par. 8-13 and 54-55). Vilcocq is not explicit about the optimization criteria relate to an input to said filter and an input to the voltage-controlled oscillator. One of ordinary skill in the art would recognize that optimization criteria of Vilcocq not only relate to the input of the voltage-controlled oscillator (i.e. output of the loop filter) but also relate to the input to the voltage-controlled oscillator. Therefore, it would have been obvious to one of ordinary skill in the art to improve the system performance of the digital synthesizer by adapting the transfer function of the filter to the linearized response of the phase locked loop variations. Also, Vilcocq is not explicit about the transfer function of the filter is an infinite impulse response. Perrott discloses digital modulation of a PLL synthesizer, wherein the filter can be an FIR or IIR filter (Col. 11,

Lines 1-14) and the FIR transfer function is more preferred comparing to an IIR transfer function filter since the filter utilizing the FIR transfer function is implemented in a Read Only Memory; and also, it is well known in the art that FIR filter is more stable and have linear phase response. On the other hand, IIR filters utilize less number of taps than FIR filters. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Perrott with Vilcocq for the reasons stated above.

As to claim 22, Vilcocq discloses all the subject matter claimed in claim 20, except for the optimization criteria includes spectral cleanliness of output of the voltage controlled oscillator. However, one of ordinary skill in the art would recognize that spectral cleanliness of the voltage-controlled oscillator is a quality parameter. Therefore, it would have been obvious to one of ordinary skill in the art to optimize the transfer function of the filter based on spectral cleanliness of the voltage-controlled oscillator in order to enhance performance of the digital modulation of a PLL synthesizer.

As to claims 30-31, Vilcocq discloses all the subject matter claimed in claim 29, except for the digital filter is a finite impulse response (FIR) or an infinite impulse response (IIR) filter. Perrott discloses digital modulation of a PLL synthesizer, wherein the filter can be an FIR or IIR filter (Col. 11, Lines 1-14) and the FIR transfer function is more preferred comparing to an IIR transfer function filter since the filter utilizing the FIR transfer function is implemented in a Read Only Memory; and also, it is well known in the art that FIR filter is more stable and have linear phase response. On the other hand, IIR filters utilize less number of taps than FIR filters. Therefore, it would have been

obvious to one of ordinary skill in the art to combine the teaching of Perrott with Vilcocq for the reasons stated above.

As to claim 32, Vilcocq further discloses that the pre-emphasis filter is an adaptive pre-emphasis filter (Fig. 2,means 18 and 26; Par. 12-13 and 54-55).

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vilcocq et al, and further in view of Hasson (US 2003/0123566).

As to claim 26, Vilcocq discloses a communication device comprising at least an antenna; a power amplifier coupled to the antenna; and a fractional-N sigma-delta modulator coupled to the power amplifier (Par. 1), the modulator including at least a filter coupled to an input of a sigma-delta converter (Fig. 2, means 15 and 18); and a fractional-N phase locked loop unit coupled to an output of the sigma-delta converter (means 11-14), wherein a transfer function of said filter is to be optimized according to predefined optimization criteria (Par. 8-13 and 54-55). Vilcocq is not explicit about the optimization criteria relate to an input to said filter and an input to the voltage-controlled oscillator. One of ordinary skill in the art would recognize that optimization criteria of Vilcocq not only relate to the input of the voltage-controlled oscillator (i.e. output of the loop filter) but also relate to the input to the voltage-controlled oscillator. Therefore, it would have been obvious to one of ordinary skill in the art to improve the system performance of the digital synthesizer by adapting the transfer function of the filter to the linearized response of the phase locked loop variations. Also, Vilcocq is not explicit about the antenna is a dipole antenna. Hasson discloses a communication device that

utilizes a diploe antenna (Fig. 1, means 108; Claim 6); a power amplifier coupled to the antenna (means 106); and a sigma-delta modulator coupled to the power amplifier (means 102). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Hasson with Vilcocq in order to transmit the modulated signal via a dipole antenna since dipole antennas show high antenna efficiency and integration flexibility.

Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vilcocq et al and Hasson, further in view of Perrott et al.

As to claims 27-28, Vilcocq and Hasson disclose all the subject matter claimed in claim 26, except for the digital filter is a finite impulse response (FIR) or an infinite impulse response (IIR) filter. Perrott discloses digital modulation of a PLL synthesizer, wherein the filter can be an FIR or IIR filter (Col. 11, Lines 1-14) and the FIR transfer function is more preferred comparing to an IIR transfer function filter since the filter utilizing the FIR transfer function is implemented in a Read Only Memory; and also, it is well known in the art that FIR filter is more stable and have linear phase response. On the other hand, IIR filters utilize less number of taps than FIR filters. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Perrott with Vilcocq and Hasson for the reasons stated above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Freshteh N. Aghdam whose telephone number is 571-272-6037. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Freshteh Aghdam
Examiner
Art Unit 2611

June 21, 2007

KEVIN BURD
PRIMARY EXAMINER